

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number (Emperor's year): 08095946 A

(43) Date of publication of application: 12 . 04 . 96

(51) Int. Cl. G06F 15/78
 G06F 9/06
 G06F 9/38
 G06F 11/22
 G06F 11/28

(21) Application number: 06252717

(71) Applicant: NEC CORP

(22) Date of filing: 22 . 09 . 94

(72) Inventor: SAKAIRI TETSUYA

(54) MICROCOMPUTER

COPYRIGHT: (C)1996,JPO

(57) Abstract:

PURPOSE: To enable a microcomputer to perform a normal operation by executing a correction program when a bug exists in a program on an incorporated ROM by performing control so as to supply a branch instruction to an instruction queue when a prefetch address to be outputted for prefetching an instruction is coincident with the contents of a register.

CONSTITUTION: When a bug exists in the program on a ROM 3, a CPU 7 continuously executes the program on the ROM 3 until a fetch pointer 1 reaches the leading address of the bug part. When the fetch pointer 1 arrives at the leading address of the bug part, namely, when the contents of the fetch pointer 1 and a register 6 are coincident with each other, a comparator circuit 5 outputs a high-level select signal 12 and a selecting circuit 8 receives the select signal 12, switches the program on the ROM 3 to the output of a branch instruction output circuit 9 and outputs the branch instruction to an instruction queue 15. The CPU 7 receives the branch instruction from the instruction queue 15 and executes it.

